

What Is Claimed Is:

1. A patch panel comprising:
 - a back plane having a front major surface and, a back major surface facing in an opposite direction;
 - a plurality of pairs of termination locations mounted to the front major surface of the back plane, each termination location including a patch cord access device defining electrical contacts connected to the back plane for electrically connecting to conductors in a patch cord;
 - a plurality of interconnect locations mounted to the front major surface of the back plane, each interconnect location defining a card edge socket with normally connected contact pairs connected to the back plane;
 - circuitry on the back plane for connecting each termination location of each pair to one of the interconnect locations.
2. The patch panel of claim 1, wherein one of the pairs of termination locations includes two RJ45 jacks.
3. The patch panel of claim 1, wherein one of the pairs of termination locations includes two insulation displacement contacts.
4. The patch panel of claim 1, wherein one of the pairs of termination locations includes an insulation displacement contact and an RJ45 jack.
5. The patch panel of claim 1, further comprising a module defining an edge contact sized for receipt in one of the card edge sockets of one of the interconnect locations.
6. The patch panel of claim 1, further comprising a power module mounted to the back major surface and electrically connected to the circuitry.

7. The patch panel of claim 1, further comprising a CPU module mounted to the back major surface and electrically connected to the circuitry.
8. A patch panel comprising:
 - a back plane having a front major surface and a back major surface;
 - a plurality of pairs of termination locations mounted to the front major surface of the back plane, each termination location including a patch cord access device defining electrical contacts connected to the back plane for electrically connecting to conductors in a patch cord;
 - a plurality of interconnect locations mounted to the front major surface of the back plane;
 - circuitry on the back plane for connecting each termination location of each pair to one of the interconnect locations;
 - at least one removable circuit module mounted to one of the interconnect locations, the removable circuit module including circuitry connected to interconnect location for connecting to one of the pairs of termination locations.
9. The patch panel of claim 8, wherein one of the pairs of termination locations includes two RJ45 jacks.
10. The patch panel of claim 8, wherein one of the pairs of termination locations includes two insulation displacement contacts.
11. The patch panel of claim 8, wherein one of the pairs of termination locations includes an insulation displacement contact and an RJ45 jack.
12. The patch panel of claim 8, further comprising a power module mounted to the back major surface and electrically connected to the circuitry.
13. The patch panel of claim 12, further comprising a CPU module mounted to the back major surface and electrically connected to the circuitry.

14. A method of patching telecommunications cables comprising:

providing a back plane including a front major surface including a plurality of pairs of cable termination locations and a plurality of interconnect locations sized to receive circuit modules, each of the interconnect locations electrically connected to one of the pairs of termination locations;

electrically connecting a plurality of pairs of telecommunications cables to the pairs of termination locations;

electrically connecting a circuit module to one of the interconnect locations, wherein the circuit module is electrically connected to one of the pairs of termination locations.

15. The method of claim 14, further comprising the steps of:

electrically connecting a power module to an opposite back major surface of the back plane;

electrically connecting a control module to the back major surface of the back plane;

wherein each of the power module and the control module are electrically connected to the interconnect locations.